REMARKS

Claims 1-3, 5-12, 15, and 21 remain in the application with claims 1 and 12 having been amended hereby and claim 13 having been canceled, without prejudice or disclaimer.

Reconsideration is respectfully requested of the rejection of claims 1-3, 5-13 and 15 under 35 U.S.C. 112, first paragraph, as not being enabled by the Specification.

Claims 1 and 12 have been amended hereby to more accurately reflect the features of the present invention. As described at page 5 of the present Specification, when a write address and a read address are the same as the data memory address, the read operation is performed in the data memory block and the write operation is performed in the sub-memory block. When the write address and the read address are the same as the data memory address, the read operation is performed in the data memory block and the write operation is performed in the sub-memory block. On the other hand, when the write address and the read address are not the same as the data memory address, the operation corresponding to the address that is the same as the data memory address is performed in the data memory and the operation of the address that is not the same as the data memory address is performed in the sub-memory block. When the write address or the read address is the same as the data memory address, the operation corresponding to the address that is the same as the data memory address is performed in the data memory block and the address that is not the same as the data memory address is performed in the sub-memory block.

Thus, as amended, it is respectfully submitted that the claim language is clearly enabled by the Specification.

Reconsideration is respectfully requested of the rejection of claims 1-3 and 5-11 under 35 U.S.C. 112, second paragraph, as being incomplete.

As noted hereinabove, claim 1 has been amended hereby to more clearly recite the manner in which the tag memory controlling unit controls the writing of data addresses into the memory blocks and the sub-memory blocks.

Accordingly, it is respectfully submitted that claim 1 is clear and definite in its recitation of the present invention and meets all requirements of 35 U.S.C. 112.

Reconsideration is respectfully requested of the rejection of claim 12 under 35 U.S.C. 112, second paragraph, as being incomplete.

Claim 12 has been amended hereby to more clearly recite the manner in which the present invention operates using the described method of performing a write operation and a read operation in a data memory block and sub-memory block.

Accordingly, it is respectfully submitted that claim 12 is clear and definite in its recitation of the present invention and meets all requirements of 35 U.S.C. 112.

Reconsideration is respectfully requested of the rejection of claims 1-3 and 5-12 under 35 U.S.C. 101 as not reciting a practical application.

On the contrary, it is respectfully submitted that an integrated circuit and method therefor that controls the writing of data into a plurality of memory blocks is clearly a practical application and even more so in today's modern society in which data being written into memories is the commonplace situation.

The claims have been amended hereby to make this data writing operation more clear so that it provides for the writing of data into data memory blocks and sub-memory blocks at the same time. The provision of a memory controlling unit, such as 210 of FIG. 2, is clearly a practical application for controlling the writing of data into the memory blocks.

Accordingly, it is respectfully submitted that the claims provide a practical application and meet the statutory requirement for a patentable invention.

Reconsideration is respectfully requested of the rejection of claims 1 and 12 under the judicially created doctrine of obviousness-type double patenting, in view of claims 14 and 18 of co-pending application 10/811,613.

Claim 14 of the pending application depends through claim 13 from claim 1. Claim 1 of the instant application is an integrated circuit. Claim 1 of the cited pending application is a method.

Therefore, it is respectfully submitted that claim 1 of the instant application and claim 1 of the cited pending application cannot cover the same subject matter, since a method claim does not infringe an apparatus claim. Claim 18 of the cited pending application depends from claim 15, which is a method claim. Claim 12 of the instant application is a method claim. Claim 15 recites the step of determining locations where write operation and read operations are to be performed. It is respectfully submitted that this does not occur in claim 12. Moreover, claim 12 has been amended hereby to include the details of the memory writing operation that are not contained in claim 18 of the pending application.

Accordingly, it is respectfully submitted that because the claims of the two applications are not co-extensive, that the obviousness-type double patenting rejection has been overcome.

Reconsideration is respectfully requested of the rejection of claims 1 and 12 under the so-called ground of non-statutory double patenting in view of claims 32, and 22 of U.S. Patent No. 6,826,088 (*Sohn, et al.*).

Initially, it is noted that it is not clear what "non-statutory double patenting" refers to.

Referring to claim 32 of *Sohn, et al.*, it will be noted that claim 1 of the instant application relates to an integrated circuit, whereas claim 32 is a method. Therefore, it is submitted that they do not cover the same subject matter.

Furthermore, claim 12 of the instant application has been amended to recite the specific relationships between the write address and read addresses relative to a data memory address. Therefore, since this feature is not suggested in claim 33 of *Sohn, et al.*, it is respectfully submitted that the claims are not co-extensive in their coverage.

In regard to claim 22 of *Sohn, et al.*, this again is a method and once again does not relate to the specifics of the reading and writing addresses relative to the data memory address, as now recited in amended claim 12.

Accordingly, it is respectfully submitted that the claims of the instant application are not co-extensive with the claims of *Sohn, et al.*

Reconsideration is respectfully requested of the rejection of claims 1-3, 8-13, and 15 under 35 U.S.C. 103(a), as being unpatentable over *Liu* in view of *Favor*.

Liu relates to a memory structure in which four sub-arrays are included and in which two effective addresses can be provided, as can be one real address. In the event that two addresses contain the same value, then these two addresses comprise a conflict and a predetermined priority resolves the conflict and the higher priority can access the sub-array. The memory is capable of being simultaneously accessed by multiple ports for access in the same cycle. The sub-arrays are of identical construction.

It is noted that *Liu* does not disclose the feature of the present invention where a write operation or a read operation is performed in a data memory block and one of the write operation

and read operation not performed is performed in a sub-memory block. *Favor* is cited to show this feature.

Favor relates to a method for reducing the number of bits when storing instruction addresses. *Favor* is cited for disclosing the memory operation wherein a store queue temporarily stores data from a storage unit so that the storage unit and the load unit operate in parallel without conflicting accesses to the data cache.

Nevertheless, *Favor* performs read and write operations in only the data cache, that is, only one memory block. More specifically, *Favor* does not perform one of a read and write operation in the data cache (216) and the other operation in the memory (130) or the second data cache (122).

Therefore, even combining *Favor* with *Liu*, it is respectfully submitted that one of ordinary skill in the art cannot know that read and write operations are respectively performed in two different memory blocks, that is, data caches of *Liu*. More specifically, even combining *Favor* with *Liu*, both read and write operations are only performed in the main memory (115) of *Liu*. On the other hand, both operations are performed in the data cache (10) of *Liu*, and both operations are performed in the second cache (110) of *Liu*.

Accordingly, by reason of the amendments made to the claims hereby, as well as the above remarks, it is respectfully submitted that a method and apparatus for inputting and outputting data using a plurality of memory blocks, as taught by the present invention and as recited in the amended claims, is neither shown nor suggested in the cited references, alone or in combination.

Notice is respectfully taken of the indication that claims 5, 7, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

It is respectfully noted that claim 21 is an independent claim that has not been separately rejected in the instant Office Action. Moreover, in view of the above, it is respectfully submitted that claims 5 and 7 are nonetheless allowable in their dependent form.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,
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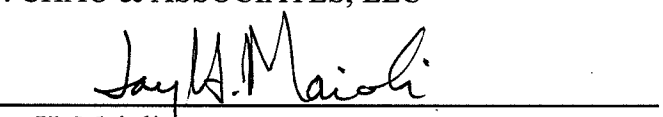

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Dated: November 2, 2007

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